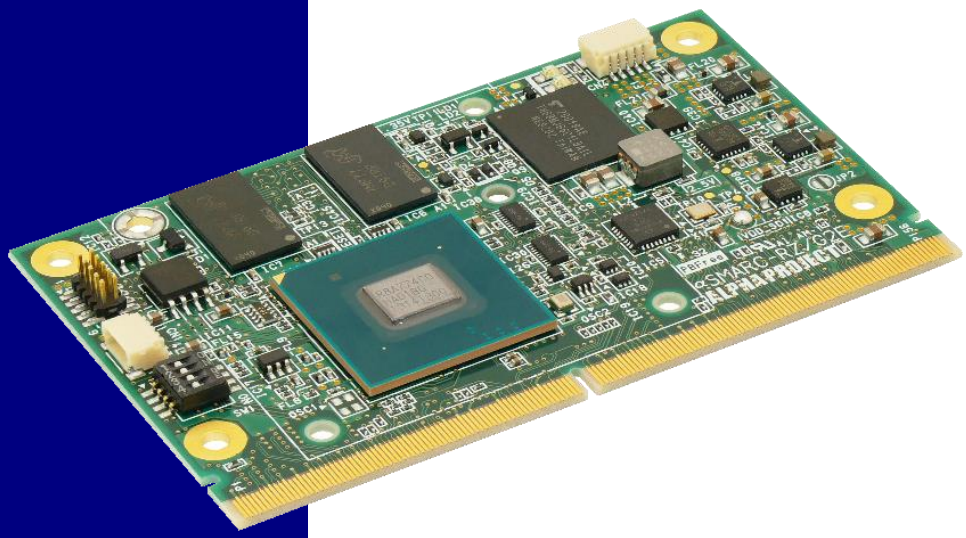
Alpha SoM Series

αSMARC-RZ/G2E

RZ/G2E System on Module

Hardware Manual

Rev 2.0



SMARC module

RoHS Compliant

ALPHA PROJECT

Important Information and Disclaimer

Thank you for purchasing an αSMARC-RZ/G2E.
Please read this manual first in order to use this module correctly.
We appreciate your continued patronage of our products.

Product Includes

This module consists of the following components. Check the contents of the package, and if anything is missing, contact the vendor from which you purchased this product.

αSMARC-RZ/G2E Product Includes

●αSMARC-RZ/G2E (with heat sink)	x1	● Manual, warranty information	x1

■ Please understand that the contents and specifications of this module are subject to change without warning.

Handling Precautions

- General consumer electronic components are used in this product, and it was designed with the intent of using it for general consumer electronic equipment. Do not use this product in applications involving human life or accidents, or applications which may cause significant property damage, such as space, aviation, medical, nuclear power, transportation, traffic, and various safety devices.
- Do not use this product in environments with extremely hot or cold temperatures or strong vibrations.
- Do not use this product in water, or environments with high humidity or excessive oil.
- Do not use this product in environments with corrosive gas, flammable gas, etc.
- Do not turn on the power when the front of the circuit board is wet or is contacting metal.
- Do not apply power that exceeds the rating.

■ Please understand that operation cannot be guaranteed in environments with excessive noise.
■ Beware that using the product in environments with continuous vibration (in vehicles, etc.) or impacts can shorten the product life or cause it to malfunction.
■ Turn off the power immediately if the product emits smoke, flame, or abnormal heat.
■ Beware that using this module in conditions that exceed the range of its specifications can cause it to malfunction.
■ Among the products and technologies listed in this manual, an export license based on the Foreign Exchange and Foreign Trade Law is required when exporting or taking out of Japan any items that fall under the regulated goods (technologies) stipulated in said law.
■ Alpha Project Co., Ltd. owns the copyright to the manual that comes with this product. It is prohibited to divert, post, transfer, or distribute this manual without permission.

Warranty

■ During the warranty period, if the product malfunctions during normal use while following precautions described in this manual, it will be covered by the warranty.
■ Regardless of whether or not the product is under warranty, Alpha Project Co., Ltd. will not compensate for any direct or indirect damage resulting from the operation of this product.
■ The warranty covers the main body of the product. The software, manuals, consumables, and packing boxes are not covered by the warranty.
■ This warranty is only valid in Japan. We do not accept requests from overseas.
■ For details on the product warranty regulations, see the attached warranty document or our website.

Reference Documents

Device and SMARC standard documents are published on the websites of various companies and organizations.
Consult them along with this manual.

■ RZ/G2E Group / Renesas Electronics
■ SMARC STANDARD (SGeT.ORG)
-SMARC Hardware Specification 2.1.1
-SMARC Design Guide Ver. 2.0

* About reference documents

- Documents and website URLs of various companies are subject to change without notice.
- Please direct inquiries about devices to the contact point of each device manufacturer.

Trademarks / License

Contents

1. Overview

1.1 Product Overview

αSMARC-RZ/G2E comes equipped with Renesas Electronics RZ/G2E MPU and is a SoM (System on Module) for mass production that conforms to the SMARC2.1 standard.

RZ/G2E is based on the ARM Cortex®-A53 dual core, has a built-in 3D graphics engine PowerVR GE8300, and supports Full HD video encoding/decoding.

Its peripheral functions include high-speed interfaces such as USB 3.0, PCI Express, Gigabit Ethernet, and many others such as LCD and AUDIO, so it is ideal for applications such as HMI for industrial use.

Its form factor conforms to the standard SMARC 2.1, and its high compatibility and extensibility make it possible to build flexible and scalable systems.

1.2 Functions and Features

■ RZ/G2E Arm® Cortex®-A53 Dual Core 1.2 GHz equipped

The ARM v8 architecture 64-bit compatible processor delivers high performance with low power consumption.

■ Supports Full HD video encoding/decoding

Supports H.264/H.265 Full HD (1920 x 1080 60 fps) encoding and decoding.

■ eMMC, DDR3-L memory equipped

Comes equipped with eMMC 8GByte for program memory and DDR3L-SDRAM 1 GByte for data memory.

■ Highly extensible interface

In addition to high-speed communication interfaces such as USB3.0, PCI Express, and Gigabit Ethernet, it has many peripheral functions such as LCD (LVDS) x 2 channels, AUDIO, camera input (MIPI CSI-2), and CAN.

■ Compliant with SMARC 2.1 standard

The module's high compatibility and extensibility make it possible to build a flexible and scalable system.

Very compact size, just 82 mm x 50 mm.

■ Supports wide temperature range

The operating temperature is -20° C to +60° C.

■ Uses Linux as the standard OS

The Verified Linux Package (Ultra Long Term Support Linux) is used to reduce the burden of software development and maintenance.

*The Verified Linux Package is provided by Renesas Electronics. Visit the Renesas Electronics website for details.

■ SMARC standard compliant carrier board is provided

A carrier board and Linux BSP are provided that allow you to start software development immediately.

The circuit diagram of the carrier board has been opened to the public, so it can be used as a reference.

1.3 About SMARC

SMARC (Smart Mobility ARChitecture) is a standard for small form factor SoM (System on Module).
Two module sizes are defined, 82 mm x 50 mm and 82 mm x 80 mm, and for signal connections we use 314-pin edge terminals mating with 0.5 mm pitch connectors.

Using SMARC SoM eliminates the need for complicated design around the CPU, which enables the user to focus on designing application-specific carrier boards, so low development costs and short time to market can be achieved.
The SMARC standard SoM and carrier board are compatible, so scalable systems can be built according to the application.

For more information on SMARC, see the SGeT (Standardization Group for Embedded Technology) home page.

SMARC Hardware Specification 2.1.1 https://www.sget.org/standards/smarc/

1.4 About Linux BSP

This module uses Linux as the standard OS.
LinuxBSP (Linux Board Support Package) is included in the development kit. For details, see our website.

1.5 Specifications Overview

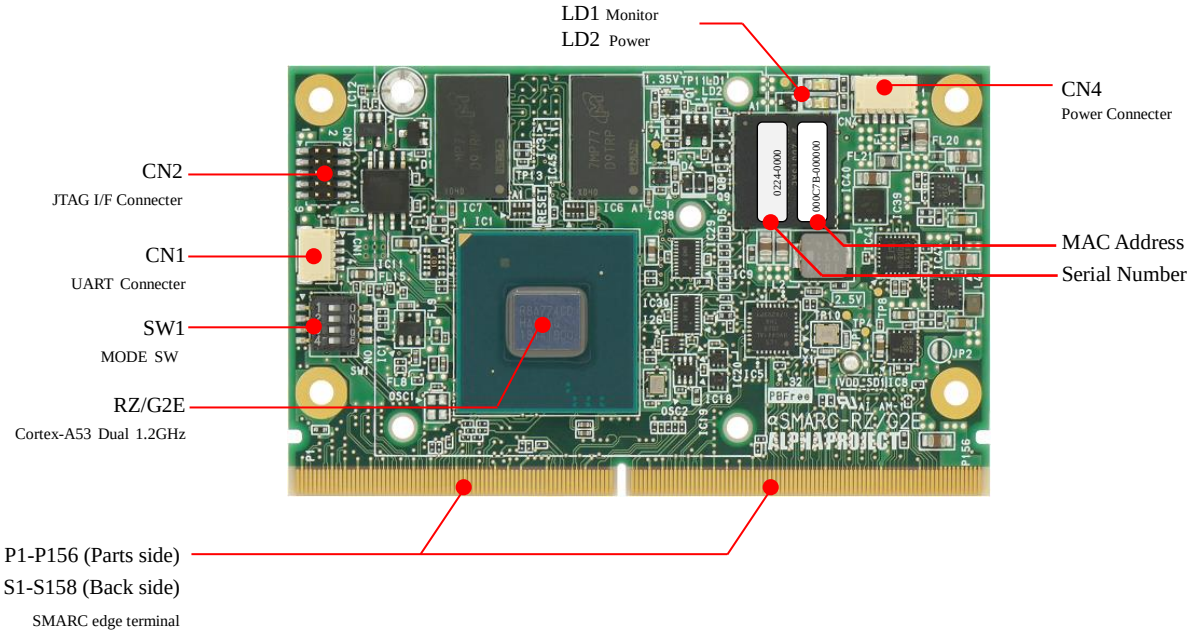
αSMARC-RZ/G2E Specifications

Function	Specifications
Form Factor	SMARC2.1 Short Size
CPU	R8A774C0HA01BG (552Pin FCBGA) Arm®Cortex®-A53 Dual Core 1.2 GHz
ROM	eMMC 8 GByte SPI FLASH 4 MByte EEPROM 2 KByte
RAM	DDR3L-1856 (928 MHz)　1 GByte / 32 bit data-bus
SMARC Interface (314 pin edge terminal)	Gigabit Ethernet ×1 USB 3.0 SuperSpeed OTG ×1 USB 2.0 High-Speed Host/Function ×2 PCI Express Rev 2.0 (1 Lane) ×1 SD-CARD ×1 LCD (LVDS) ×2 CAMERA (MIPI CSI-2) ×1 UART ×3 CAN (FD Support) ×2 AUDIO I2S ×1 SPI ×1 I2C ×3 GPIO ×14
RTC	Maximum daily difference ±2 seconds Backup with external power supply
LED	Monitor LED ×1 Power LED ×1
UART	UART Connector UART (TTL) 1 port
JTAG	JTAG Connector CoreSight half pitch 10 pin (5p × 2 rows)
Heat Sink	Dedicated product installed
Power Supply	DC 5.0 V ±5%
Current Consumption	Max 10 W
Use Environment Conditions	Temperature: -20 to +60˚ C (no condensation)
Dimensions	82 mm (W) × 50 mm (D)
Circuit Board	FR-4 (UL94-V0)
Environmental Support	RoHS directive (2015/863/EU)
Preinstalled OS	CIP Linux 4.19　*As of October 2, 2023

Table 1.5-1 Hardware specifications

1.6 External Specifications

[Parts]



When a heat sink is attached

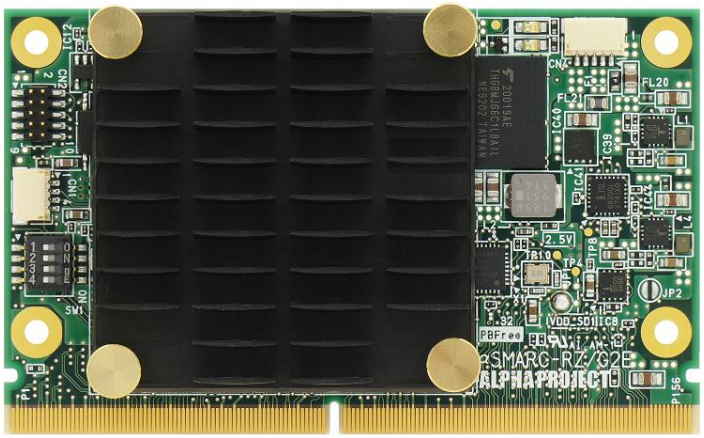


Fig 1.6-1 Appearance

1.7 Circuit Configuration

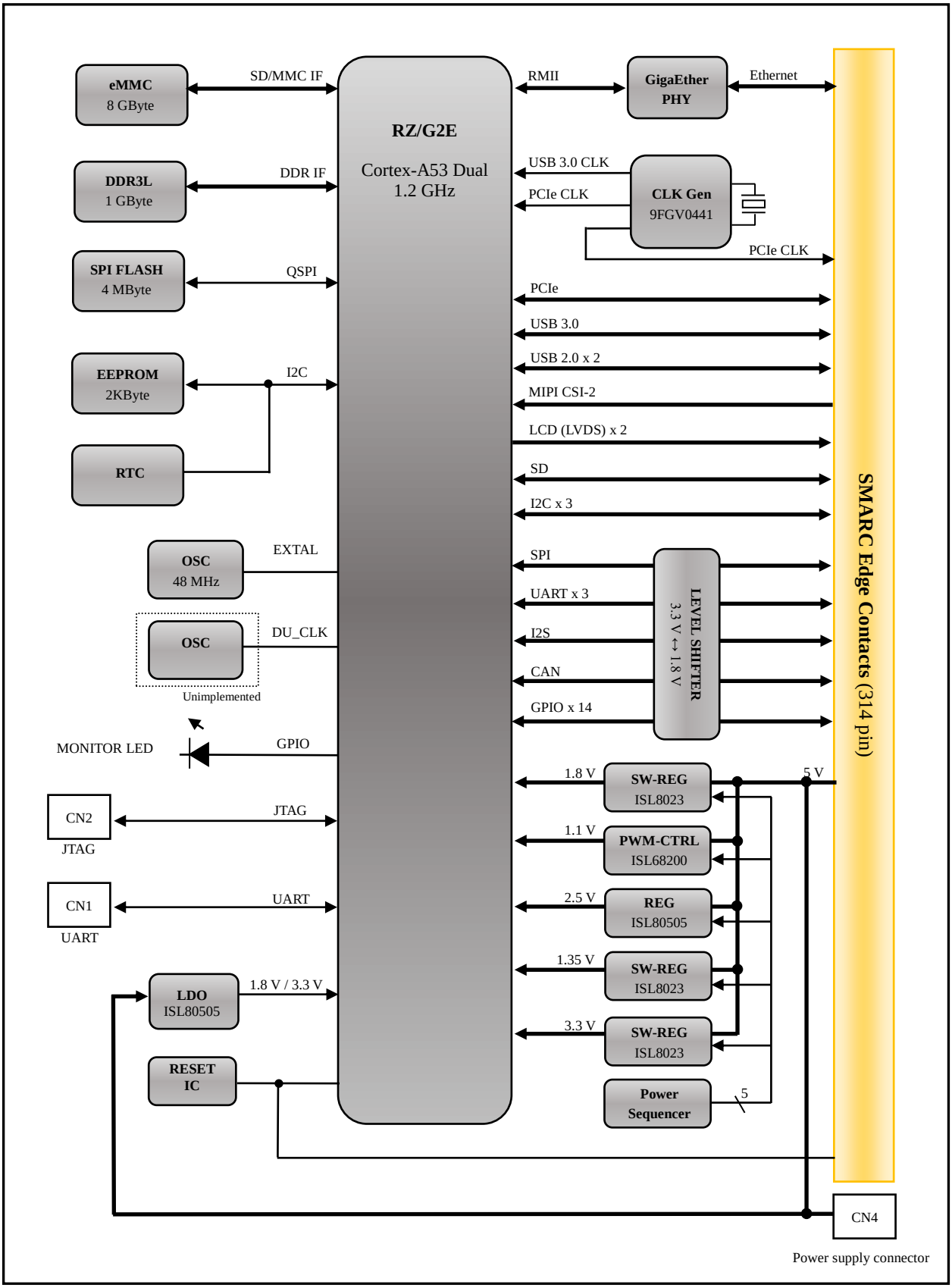


Fig 1.7-1 αSMARC-RZ/G2E configuration block diagram

The main devices and parts used in this module are as follows.

For device specifications, see the website of each device manufacturer.

Product Function	Model / Manufacturer	Specifications	Remarks
CPU	R8A774C0HA01BG / Renesas	ARM Cortex-A53 Dual	
eMMC	THGBMJG6C1L / Kioxia	64 Gbit eMMC	*1
DDR3L	MT41K256M16 / Micron	4 Gbit DDR3L Memory	*1
SPI FLASH	MX25L3235E / Macronix	32 Mbit QSPI FLASH	*1
RealTimeClock	S-35390A / ABLIC	RealTimeClock	
Ethernet PHY	KSZ9131RNXI / Microchip	Gigabit Ethernet Transceiver	
Clock Generator	9FGV0441AKLF / Renesas	PCIe Clock Generator	
Power	ISL8023IRTAJZ-T7A / Renesas	SwitchBuck-Reg	
Power	ISL68200IRZ-T7A / Renesas	PWM Controller	
Power	ISL80505IRAJZ-T7A / Renesas	LowDrop-Reg	

Table 1.7-2 Main devices

Connector Number	Connector Model / Manufacturer	Application	Remarks
CN1	SM4B-SRSS-TB / JST	UART Connecter	
CN2	HEADER 10p (5px2) 1.27 mm Pitch	JTAG Connector	
CN4	SM05B-SRSS-TB / JST	Power Connecter	

Table 1.7-3 Connector List

*1 Please note that parts may be changed to equivalent products without notice.

1.8 Address Map

Address	Area
H'00_00000000	Legacy (DDR0 shadow A) *1
H'01_00000000	Reserved
H'02_00000000	Reserved
H'03_00000000	Reserved
H'04_00000000 H'04_3FFFFFFF	DDR0 Area DDR3L 1 GByte
H'05_40000000	DDR3L Mirror
H'05_00000000	Reserved
H'06_00000000	Reserved
H'07_00000000	Reserved
H'08_00000000	DDR0 Area shadow B
H'09_00000000	Reserved
H'0A_00000000	Reserved
H'0B_00000000	Reserved
H'0C_00000000	DDR0 Area shadow C
H'0D_00000000	Reserved
H'0E_00000000	Reserved
H'0F_00000000	Reserved
H'10_00000000	Reserved
H'11_00000000	Reserved
H'12_00000000	Reserved
H'13_00000000	Reserved
H'14_00000000	Reserved
H'15_00000000	Reserved
H'18_00000000	uTLB (IPMMU slave) ch0
H'1C_00000000	Reserved
H'20_00000000	Reserved
H'30_00000000	Reserved
H'FF_00000000	Reserved

Fig 1.8-1 Address Map

*1 Internal registers are assigned to the Legacy Area.
For details on the address map, see the "RZ/G Series 2nd Generation User's Manual: Hardware".

2. Functions

2.1 CPU

This module is equipped with RZ/G2E MPU manufactured by Renesas Electronics.
It is based on the ArmV8 architecture 64 bit compatible processor Arm® Cortex-A53 dual core, and in addition to advanced graphics functions such as a 3D graphics engine and video encoder, it also supports high-speed interfaces such as Gigabit Ethernet, USB 3.0, PCI Express, and MIPI CSI-2.
For detailed functions of RZ/G2E, see the Renesas Electronics product page and device datasheet.

RZ/G2E product page (Renesas Electronics) RZ/G2E microprocessor

2.2 MEMORY

2.2.1 eMMC NAND Flash

This module is equipped with 8 GByte eMMC NAND Flash.
It is connected to the MMC interface (SDHI3) of RZ/G2E and can be used as a boot device.
Bandwidth is up to 400 MB/s in HS400 mode.

2.2.2 DDR3L SDRAM

This module is equipped with 1 GByte DDR3L SDRAM.
It is connected to the RZ/G2E's External BUS Controller via a 32 bit bus.
The clock has a maximum of 928 MHz (DDR3L-1856), and the bandwidth is up to 7424 MB/s.

2.2.3 SPI FLASH

This module has a 4 MByte SPI FLASH.
It is connected to the RZ/G2E SPI Multi I/O Bus Controller (QSPI0) and can be used as a boot device when updating firmware.

2.3 Other

2.3.1 RTC

This module is equipped with RTC (Real Time Clock).

It can be backed up from VDD_RTC of the SMARC interface.

Function	Specifications
RTC	S-35390A (ABLIC) Current consumption: 0.25 uA Typ Maximum daily difference ±2 seconds

Table 2.3-1 Overview of RTC specifications

2.3.2 EEPROM

This module is equipped with 2 KByte EEPROM.

It is used to store parameters such as MAC addresses. The MAC address assigned by our company is written at time of shipment.

2.3.3 I2C Control Device

EEPROM, RTC, Clock Generate, and PWM Controller are connected to RZ/G2E's I2C interface and can be controlled.

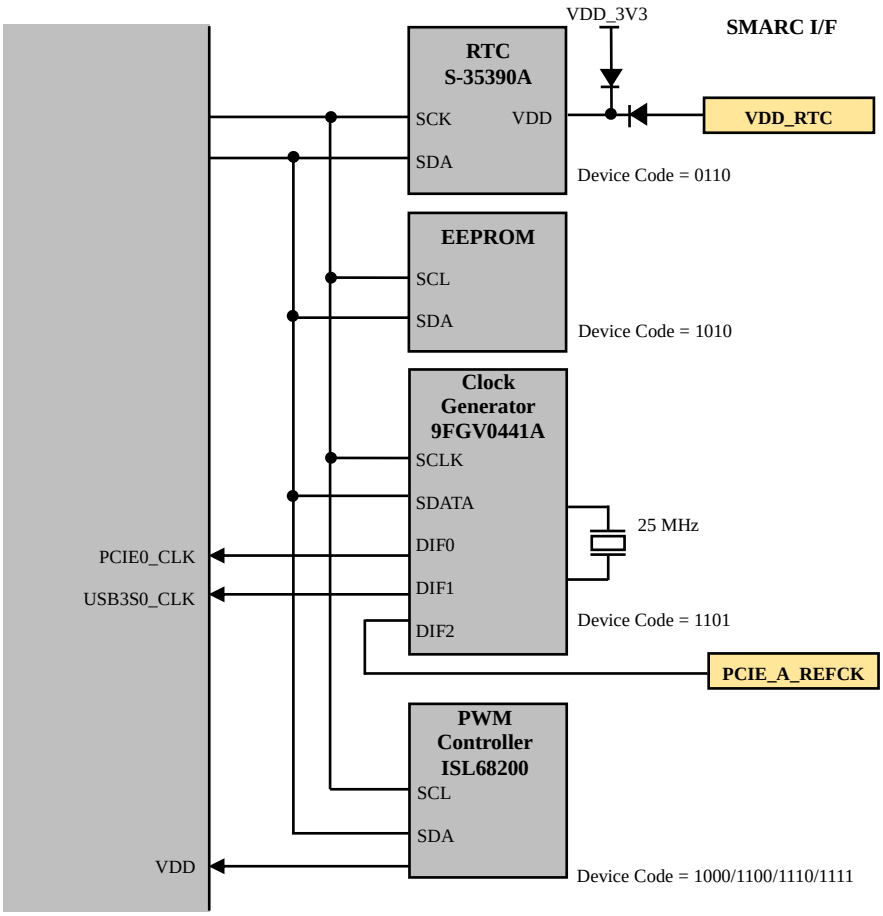


Fig 2.3-2 I2C control device circuit connection configuration

2.4 SMARC Interface

2.4.1 Interface Terminal

This module complies with SMARC standard 2.1.

The connection with the carrier board of the SMARC standard module is an edge terminal, and the shape is suitable for MXM 3.0 connectors.

The assignment of pin numbers is unique to the SMARC standard, with P1-P156 arranged on the front side and S1-S158 arranged on the back side, for a total of 314 pins.

Module front (parts side) **Module rear (back side)**

Fig 2.4-1 SMARC edge terminal layout

2.4.2 Supported Functions

The SMARC standard defines the level of support required for each function, and they are categorized as follows.

" shall"	Must
"should"	Recommended
"May"	Not often used option
"Alternate"	Options shared with another use

This module supports the following functions and signals.

Table 2.4-2 Function list

o: Supported -- : Not supported

Function	Channel	SMARC requirement	αSMARC-RZ/G2E	Remarks
LVDS LCD	LVDS0	*Should*	O	24 bit Single or Dual
	LVDS1	*May*	O	
HDMI	HDMI	*Should*	--	
Display Port	DP0	*May*	--	
	DP1	*May*	--	
Camera	CSI0	*May*	--	
	CSI1	*Should*	O	
SDIO	SDIO	*Should*	O	
SPI	SPI0	*Should*	O	
	eSPI1	*Should*	--	
Audio	I2S0	*Should*	O	
	HDA	*Should*	--	

I2C	Power Management	***Shall***	O	
	General Purpose	***Shall***	O	
	CAMERA	*May*	O	Shared with General Purpose
	LCD	*May*	O	
Serial Ports	SER0	***Shall***	O	
	SER1	***Shall***	O	
	SER2	*Should*	O	
	SER3	*Should*	--	
CAN Bus	CAN0	*May*	O	
	CAN1	*May*	O	
USB	USB0	***Shall***	O	Function (exclusive with USB1)
	USB1	***Shall***	O	Host (exclusive with USB0)
	USB2	*May*	--	
(Super Speed)	USB2 SS	*May*	--	
	USB3	*May*	O	OTG
(Super Speed)	USB3 SS	*May*	O	OTG
	USB4	*May*	--	
	USB5	*May*	--	
PCI Express	PCIe_A	*Should*	O	
	PCIe_B	*May*	--	
	PCIe_C	*May*	--	
	PCIe_D	*May*	--	
Serial ATA	SATA	*Should*	--	
Gigabit Ethernet	GBE0	*Should*	O	
	GBE1	*May*	--	
Watchdog	WDT Out	*Should*	--	
GPIO	GPIO[0:11]	***Shall***	O	
	GPIO[12:13]	*Should*	O	
Management	CARRIER_PWR_ON	***Shall***	O	
	VIN_PWR_BAD#	***Shall***	O	
	CARRIR_STBY#	*Should*	--	
	POWER_BTN#	*Should*	O	
	RESET_IN#	*Should*	O	
	RESET_OUT#	*Should*	O	
	CHARGING#	*Should*	--	
	CHARGE_PRSNT#	*Should*	--	
	BATLOW#	*Should*	--	
	SLEEP#	*Should*	--	
	SMB_ALERT#	*Should*	--	
	TEST#	*Should*	O	
BootSelect	BOOT_SEL[0:2]#	***Shall***	O	
ForceRecov	FORCE_RECOV#	*Should*	O	
RTC	VDD_RTC	*Should*	O	
POWER	VDD_IN	***Shall***	O	
	GND	***Shall***	O	

2.4.3 Signal Assignment

The signal assignments for the SMARC interface are shown in the following table.

- "N.C" in the signal name indicates Not Connected.
- "P.U" and "P.D" indicate pull-up or pull-down within SoM.
- "O.D" indicates open drain.
- "x" in voltage indicates it conforms to the standard of each interface.
- VDD_IO can be set to 1.8 V (standard) or 3.3 V. For details, see "2.5.2 VDD_IO Settings".

For definitions of each signal in the SMARC standard, see the SMARC standard specification.

SMARC Hardware Specification 2.1.1 https://www.sget.org/standards/smarc/

Table 2.4-3 SMARC interface signal assignment

No.	Signal Name	Input/ Output	Voltage	Remarks
P1	N.C			
P2	GND		GND	
P3	CSI1_CK+	In	x	
P4	CSI1_CK-	In	x	
P5	N.C			
P6	N.C			
P7	CSI1_RX0+	In	x	
P8	CSI1_RX0-	In	x	
P9	GND		GND	
P10	CSI1_RX1+	In	x	
P11	CSI1_RX1-	In	x	
P12	GND		GND	
P13	N.C			
P14	N.C			
P15	GND		GND	
P16	N.C			
P17	N.C			
P18	GND		GND	
P19	GBE0_MDI3-	I/O	x	
P20	GBE0_MDI3+	I/O	x	
P21	GBE0_LINK100#	Out	3.3 V O.D	
P22	GBE0_LINK1000#	Out	3.3 V O.D	
P23	GBE0_MDI2-	I/O	x	
P24	GBE0_MDI2+	I/O	x	
P25	GBE0_LINK_ACT#	Out	3.3 V O.D	
P26	GBE0_MDI1-	I/O	x	
P27	GBE0_MDI1+	I/O	x	
P28	GBE0_CTREF	Out	x	
P29	GBE0_MDI0-	I/O	x	
P30	GBE0_MDI0+	I/O	x	
P31	N.C	In	VDD_IO	P.U 10K
P32	GND		GND	
P33	SDIO_WP	In	3.3 V	P.U 10K
P34	SDIO_CMD	I/O	3.3 V/1.8 V	P.U 47K
P35	SDIO_CD#	In	3.3 V	P.U 10K
P36	SDIO_CK	Out	3.3 V/1.8 V	P.U 47K

No.	Signal Name	Input/ Output	Voltage	Remarks
S1	I2C_CAM1_CK	Out	VDD_IO	P.U 2.2k
S2	I2C_CAM1_DAT	Out	VDD_IO	P.U 2.2k
S3	GND		GND	
S4	N.C			
S5	N.C			
S6	CAM_MCK	Out	VDD_IO	
S7	N.C			
S8	N.C			
S9	N.C			
S10	GND		GND	
S11	N.C			
S12	N.C			
S13	GND		GND	
S14	N.C			
S15	N.C			
S16	GND		GND	
S17	N.C			
S18	N.C			
S19	N.C			
S20	N.C			
S21	N.C			
S22	N.C			
S23	N.C			
S24	N.C			
S25	GND		GND	
S26	N.C			
S27	N.C			
S28	N.C			
S29	N.C			
S30	N.C			
S31	N.C			
S32	N.C			
S33	N.C			
S34	GND		GND	
S35	N.C			
S36	N.C			

P37	SDIO_PWR_EN	Out	3.3 V	P.U 47k
P38	GND		GND	
P39	SDIO_D0	I/O	3.3 V/1.8 V	P.U 47k
P40	SDIO_D1	I/O	3.3 V/1.8 V	P.U 47k
P41	SDIO_D2	I/O	3.3 V/1.8 V	P.U 47k
P42	SDIO_D3	I/O	3.3 V/1.8 V	P.U 47k
P43	SPI0_CS0#	Out	VDD_IO	
P44	SPI0_CK	Out	VDD_IO	
P45	SPI0_DIN	In	VDD_IO	
P46	SPI0_DO	Out	VDD_IO	
P47	GND		GND	
P48	N.C			
P49	N.C			
P50	GND		GND	
P51	N.C			
P52	N.C			
P53	GND		GND	
P54	N.C			
P55	N.C			
P56	N.C			
P57	N.C			
P58	N.C			
P59	GND		GND	
P60	USB0+	I/O	x	
P61	USB0-	I/O	x	
P62	USB0_EN_OC#	I/O	3.3 V O.D	P.U 10k
P63	USB0_VBUS_DET	In	5 V	P.D 100k
P64	N.C			
P65	USB1+	I/O	x	
P66	USB1-	I/O	x	
P67	USB1_EN_OC#	I/O	3.3 V O.D	P.U 10k
P68	GND		GND	
P69	N.C			
P70	N.C			
P71	N.C		3.3 V	P.U 10k
P72	N.C			
P73	N.C			
P74	USB3_EN_OC#	I/O	3.3 V O.D	P.U 10k
P75	PCIE_A_RST#	Out	3.3 V	P.U 47k
P76	N.C		3.3 V	P.U 10k
P77	N.C			
P78	N.C			
P79	GND		GND	
P80	N.C			
P81	N.C			
P82	GND		GND	
P83	PCIE_A_REFCK+	Out	x	
P84	PCIE_A_REFCK-	Out	x	
P85	GND		GND	
P86	PCIE_A_RX+	In	x	
P87	PCIE_A_RX-	In	x	
P88	GND		GND	
P89	PCIE_A_TX+	Out	x	
P90	PCIE_A_TX-	Out	x	

S37	USB3_VBUS_DET	In	5 V	P.D 100k
S38	AUDIO_MCK	Out	VDD_IO	
S39	I2S0_LRCK	I/O	VDD_IO	
S40	I2S0_SDOUT	Out	VDD_IO	
S41	I2S0_SDIN	In	VDD_IO	
S42	I2S0_CK	I/O	VDD_IO	
S43	N.C			
S44	N.C			
S45	N.C			
S46	N.C			
S47	GND		GND	
S48	I2C_GP_CK	Out	VDD_IO	P.U 2.2k
S49	I2C_GP_DAT	I/O	VDD_IO	P.U 2.2k
S50	N.C			
S51	N.C			
S52	N.C			
S53	N.C			
S54	N.C			
S55	N.C		3.3 V	P.U 10k
S56	N.C			
S57	N.C			
S58	N.C			
S59	N.C			
S60	N.C			
S61	GND		GND	
S62	USB3_SSTX+	Out	x	
S63	USB3_SSTX-	Out	x	
S64	GND		GND	
S65	USB3_SSRX+	In	x	
S66	USB3_SSRX-	In	x	
S67	GND		GND	
S68	USB3+	I/O	x	
S69	USB3-	I/O	x	
S70	GND		GND	
S71	N.C			
S72	N.C			
S73	GND		GND	
S74	N.C			
S75	N.C			
S76	N.C			
S77	N.C			
S78	N.C			
S79	N.C			
S80	GND		GND	
S81	N.C			
S82	N.C			
S83	GND		GND	
S84	N.C			
S85	N.C			
S86	GND		GND	
S87	N.C			
S88	N.C			
S89	GND		GND	
S90	N.C			

P91	GND		GND	
P92	N.C			
P93	N.C			
P94	GND		GND	
P95	N.C			
P96	N.C			
P97	GND		GND	
P98	N.C			
P99	N.C			
P100	GND		GND	
P101	N.C			
P102	N.C			
P103	GND		GND	
P104	N.C			
P105	N.C		VDD_IO	P.U 100k
P106	N.C		VDD_IO	P.U 100k
P107	N.C			
P108	GPIO0	I/O	VDD_IO	P.U 470k
P109	GPIO1	I/O	VDD_IO	P.U 470k
P110	GPIO2	I/O	VDD_IO	P.U 470k
P111	GPIO3	I/O	VDD_IO	P.U 470k
P112	GPIO4	I/O	VDD_IO	P.U 470k
P113	GPIO5	I/O	VDD_IO	P.U 470k
P114	GPIO6	I/O	VDD_IO	P.U 470k
P115	GPIO7	I/O	VDD_IO	P.U 470k
P116	GPIO8	I/O	VDD_IO	P.U 470k
P117	GPIO9	I/O	VDD_IO	P.U 470k
P118	GPIO10	I/O	VDD_IO	P.U 470k
P119	GPIO11	I/O	VDD_IO	P.U 470k
P120	GND		GND	
P121	I2C_PM_CK	I/O	VDD_IO	P.U 2.2K
P122	I2C_PM_DAT	I/O	VDD_IO	P.U 2.2K
P123	BOOT_SEL0#	In	VDD_IO	P.U 1.5k
P124	BOOT_SEL1#	In	VDD_IO	P.U 1.5k
P125	BOOT_SEL2#	In	VDD_IO	P.U 1.5k
P126	RESET_OUT#	Out	VDD_IO	
P127	RESET_IN#	In	3.3 V	P.U 10k
P128	POWER_BTN#	In	VDD_IN	P.U 10k
P129	SER0_TX	Out	VDD_IO	
P130	SER0_RX	In	VDD_IO	P.U 100k
P131	SER0_RTS#	Out	VDD_IO	
P132	SER0_CTS#	In	VDD_IO	P.U 100k
P133	GND		GND	
P134	SER1_TX	Out	VDD_IO	
P135	SER1_RX	In	VDD_IO	P.U 100k
P136	SER2_TX	Out	VDD_IO	
P137	SER2_RX	In	VDD_IO	P.U 100k
P138	SER2_RTS#	Out	VDD_IO	
P139	SER2_CTS#	In	VDD_IO	
P140	N.C			
P141	N.C			
P142	GND		GND	
P143	CAN0_TX	Out	VDD_IO	
P144	CAN0_RX	In	VDD_IO	P.U 470k

S91	N.C			
S92	GND		GND	
S93	N.C			
S94	N.C			
S95	N.C			
S96	N.C			
S97	N.C			
S98	N.C			
S99	N.C			
S100	N.C			
S101	GND		GND	
S102	N.C	Out		
S103	N.C	Out		
S104	USB3_OTG_ID	In	3.3 V	
S105	N.C			
S106	N.C			
S107	LCD1_BKLT_EN	Out	VDD_IO	P.D 470k
S108	LVDS1_CK+	Out	x	
S109	LVDS1_CK-	Out	x	
S110	GND		GND	
S111	LVDS1_0+	Out	x	
S112	LVDS1_0-	Out	x	
S113	N.C			
S114	LVDS1_1+	Out	x	
S115	LVDS1_1-	Out	x	
S116	LCD1_VDD_EN	Out	VDD_IO	P.D 470k
S117	LVDS1_2+	Out	x	
S118	LVDS1_2-	Out	x	
S119	GND		GND	
S120	LVDS1_3+	Out	x	
S121	LVDS1_3-	Out	x	
S122	LCD1_BKLT_PWM	Out	VDD_IO	P.D 470k
S123	GPIO13	I/O	VDD_IO	P.U 470k
S124	GND		GND	
S125	LVDS0_0+	Out	x	
S126	LVDS0_0-	Out	x	
S127	LCD0_BKLT_EN	Out	VDD_IO	P.D 470k
S128	LVDS0_1+	Out	x	
S129	LVDS0_1-	Out	x	
S130	GND		GND	
S131	LVDS0_2+	Out	x	
S132	LVDS0_2-	Out	x	
S133	LCD0_VDD_EN	Out	VDD_IO	P.D 470k
S134	LVDS0_CK+	Out	x	
S135	LVDS0_CK-	Out	x	
S136	GND		GND	
S137	LVDS0_3+	Out	x	
S138	LVDS0_3-	Out	x	
S139	I2C_LCD_CK	Out	VDD_IO	P.U 2.2k
S140	I2C_LCD_DAT	I/O	VDD_IO	P.U 2.2k
S141	LCD0_BKLT_PWM	Out	VDD_IO	P.D 470k
S142	GPIO12	I/O	VDD_IO	P.U 470k
S143	GND		GND	
S144	N.C			

P145	CAN1_TX	Out	VDD_IO	
P146	CAN1_RX	In	VDD_IO	P.U 470k
P147	VDD_IN	In	4.75 - 5.25 V	
P148	VDD_IN	In	4.75 - 5.25 V	
P149	VDD_IN	In	4.75 - 5.25 V	
P150	VDD_IN	In	4.75 - 5.25 V	
P151	VDD_IN	In	4.75 - 5.25 V	
P152	VDD_IN	In	4.75 - 5.25 V	
P153	VDD_IN	In	4.75 - 5.25 V	
P154	VDD_IN	In	4.75 - 5.25 V	
P155	VDD_IN	In	4.75 - 5.25 V	
P156	VDD_IN	In	4.75 - 5.25 V	

S145	N.C		VDD_IO	P.U 10k
S146	PCIE_WAKE#	In	3.3 V	P.U 10k
S147	VDD_RTC	In	2.0 - 3.25 V	
S148	N.C			
S149	N.C			
S150	VIN_PWR_BAD#	In	VDD_IN	P.U 10k
S151	N.C			
S152	N.C			
S153	N.C		VDD_IO	P.U 10k
S154	CARRIER_PWR_ON	Out	VDD_IO	
S155	FORCE_RECOV#	In	VDD_IO	P.U 10k
S156	N.C			
S157	TEST#	In	1.8 V	P.U 1.5k
S158	GND		GND	

2.4.4 DC Characteristics

Each signal is compliant with common 1.8 V CMOS or 3.3 V CMOS.

Item	Symbol	Min	Max	UNIT
VDD_IN				
Power Supply	VDD_IN	4.75	5.25	V
1.8 V (SDIO)				
High-Level Output Voltage	VOH	1.4		V
Low-Level Output Voltage	VOL		0.45	V
High-Level Input Voltage	VIH	1.27	2.1	V
Low-Level Input Voltage	VIL	-0.3	0.58	V
3.3 V				
High-Level Output Voltage	VOH	2.4	3.6	V
Low-Level Output Voltage	VOL		0.4	V
High-Level Input Voltage	VIH	2.0	3.6	V
Low-Level Input Voltage	VIL	-0.3	0.4	V
VDDIO (1.8 V or 3.3 V)				
High-Level Output Voltage	VOH	VDDIO × 0.65	VDDIO - 0.4	V
Low-Level Output Voltage	VOL		0.4	V
High-Level Input Voltage	VIH	VDDIO × 0.65	VDDIO + 0.3	V
Low-Level Input Voltage	VIL	0	VDDIO × 0.35	V

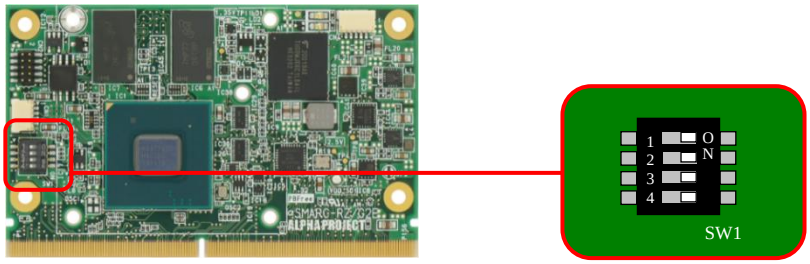
Table 2.4-4 SMARC interface DC characteristics

2.5 Settings

2.5.1 CPU Operating Settings

The CPU operating mode is set by SW1.

Normally there is no problem with the default settings, but you can change the settings as necessary.



SW1	Settings	Factory settings	OFF	ON
-1	JTAG MODE	ON	--	**Core Sight**
-2	ARM v8 initial run state	ON	Arch32	**Arch64**
-3	System Clock SSCG Enabled/Disabled	ON	SSCG OFF	**SSCG ON**
-4	Boot Mode	ON	SPI FLASH	**eMMC / SPI_FLASH *1**

*1 Switches depending on the FORCE_RECOV# signal status. See “4.2.2 FORCE_RECOV”.

Fig 2.5-1 CPU operation settings

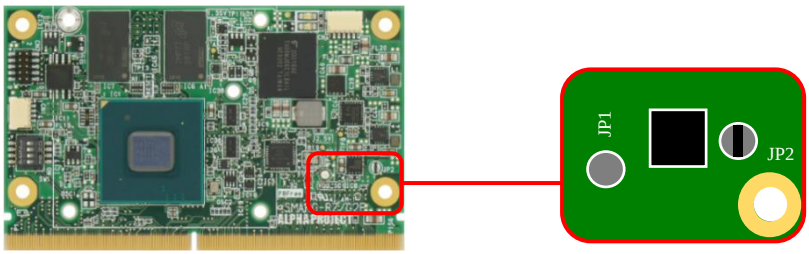
2.5.2 VDD_IO Settings

The I/O voltage of the signal of the edge terminal of SMARC is normally defined at 1.8 V.

However, when designing carrier boards, in many cases it is better in terms of cost and performance to design the I/O voltage at 3.3 V.

With this module, the I/O voltage of some signals can be switched to 3.3 V by setting VDD_IO.

Note that the 3.3 V setting is not normal with the SMARC standard.



JP1	JP2	VDD_IO voltage	Remarks
Short circuit	Open	**1.8 V (SMARC standard)**	Factory settings
Open	Short circuit	3.3 V	
Other		Settings not possible	Do not make this setting. Doing so can cause damage.

Fig 2.5-2 VDD_IO settings

2.6 LED Indicator

This module has one monitor LED (green) and one power LED (red).

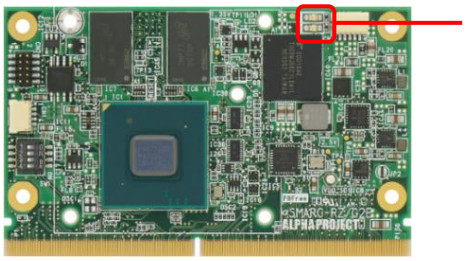
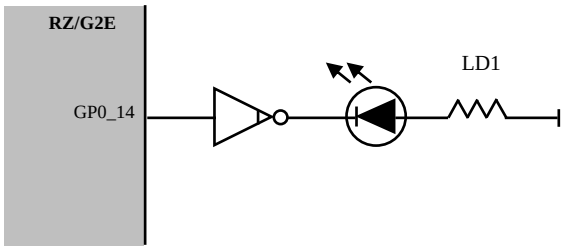


Fig 2.6-1 LED Position

2.6.1 Monitor LED

Monitor LED is controlled from the port of RZ/G2E.

Software can turn the LED on or off at any time.



GP0_14 output	LD1
HIGH	Light On
LOW	Light Off

Fig 2.6-2 Monitor LED Circuit Configuration

2.6.2 Power LED

The power supply LED lights up when the module powers on.

Power supply status	LD2
ON	Light On
OFF	Light Off

Table 2.6-3 Power LED status

2.7 UART Connector

CN1 is connected to the RZ/G2E UART interface signal.

It is assumed to be used for monitoring programs and for testing with individual modules.

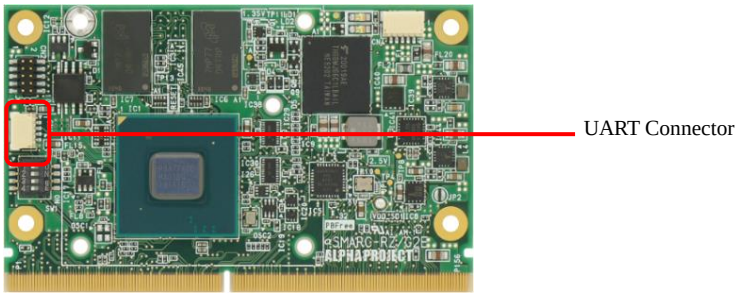
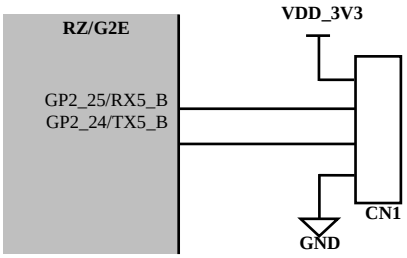


Fig 2.7-1 UART Connector Position



No.	Signal Name	Voltage Level
1	VDD_3V3	3.3 V
2	GP2_25/RX5_B	3.3 V
3	GP2_24/TX5_B	3.3 V
4	GND	GND

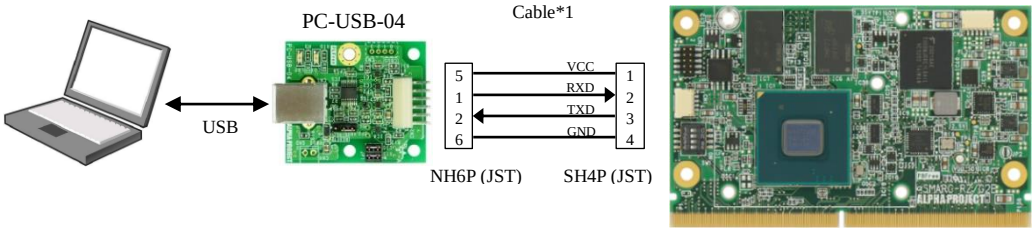
UART Connector (CN1) pin assignment

Fig 2.7-2 UART Connector circuit configuration and pin assignment

Example of connecting to a PC using PC-USB-04

To connect to a PC, use our company's product "PC-USB-04" or a commercially available UART/USB signal conversion unit.

The following is an example of connection when using PC-USB-04.



*1 A cable is not included with the product. Please prepare one yourself.

Fig 2.7-3 Connection example with PC-USB-04

2.8 JTAG Connector

CN2 is connected to the RZ/G2E JTAG interface signal.

The connector uses a 1.27 mm pitch 10 pin, and by connecting a JTAG emulator, you can debug programs and write to flash ROM.

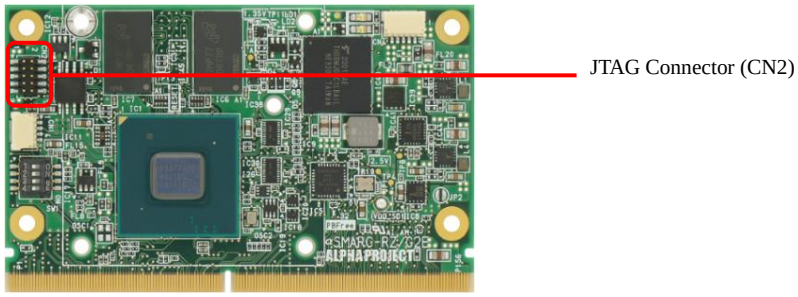


Fig 2.8-1 JTAG Connector Position

P.U : Pull-Up P.D : Pull-Down

No.	Signal Name	Remarks	No.	Signal Name	Remarks
1	VDD	1.8 V	2	TMS	P.U 10K
3	GND		4	TCK	P.U 10K
5	GND		6	TDO	P.U 10K
7	N.C		8	TDI	P.U 10K
9	TRST#	P.D 1K	10	PRESET#	RZ/G2E PRESET# and connection

Table 2.8-2 JTAG Connector Pin Assignment

ARM core JTAG interfaces include 10 pin (half pitch), 20 pin (full pitch), 20 pin (half pitch), etc. When connecting to this board, use 10 pin (half pitch).

2.9 Power Supply Connector

CN4 is a connector for power supply input.

The power supply is normally input from the edge terminal, so the power connector is not used.

It is used when operating the module independently for purposes such as testing.

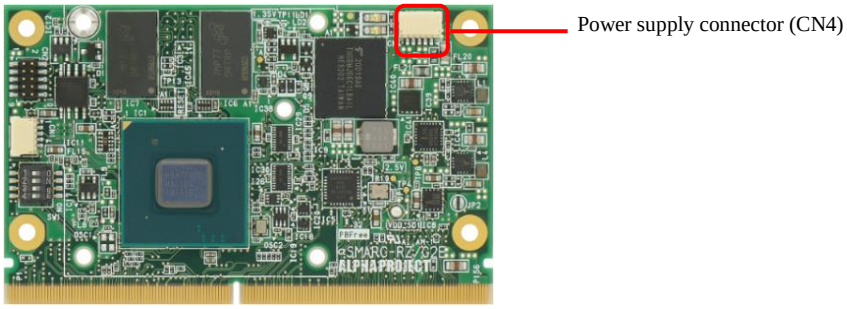
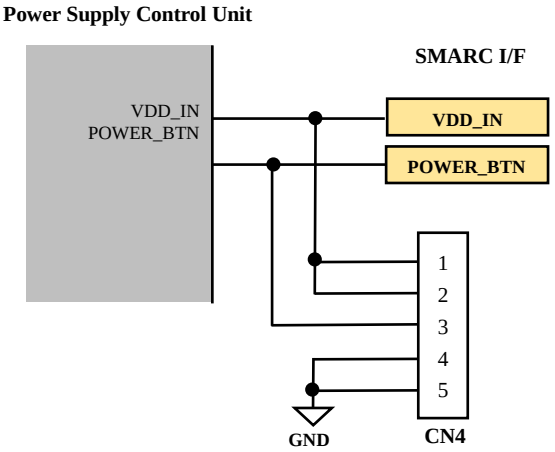


Fig 2.9-1 Power supply connector Position



No.	Signal Name	Remarks
1	VDD_IN	5 V
2	VDD_IN	5 V
3	PWR_BTN	Low Active
4	GND	
5	GND	

Power supply connector (CN4) pin assignment

Fig 2.9-2 Power supply connector circuit configuration and pin assignment

3. Interface Function Details

3.1 LVDS LCD

LVDS LCD supports Single Link x 2 channels or Dual Link x 1 channel.
It is connected to LVDS Interface of RZ/G2E and controlled with the Display Unit.
The supported output format is RGB888/YCbCr422, and the 3D accelerator and Video Codec enable rich graphics display that also support Full HD video.
Rich graphics display is possible.

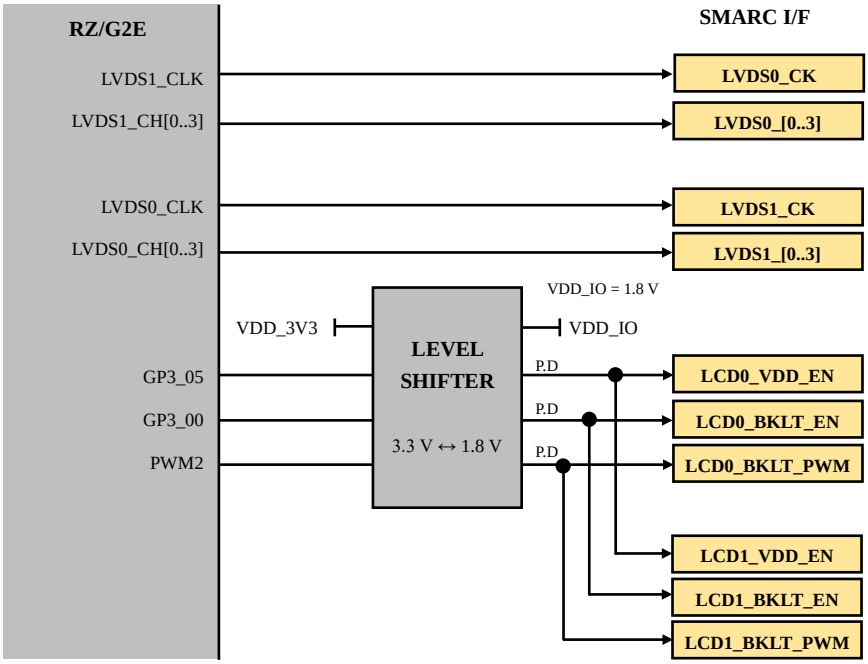


Fig 3.1-1 LCD LVDS circuit connection configuration

Please note that the connections have been interchanged for LVDS0/1 of RZ/G2E and the LVDS0/1 of the SMARC interface.

The LCD power supply and back light control signal are relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

3.2 Gigabit Ethernet

Gigabit Ethernet (100/1000BASE) x 1 port is supported.

It is controlled by RZ/G2E EtherAVB-IF (E-MAC) and external PHY. RZ/G2E and PHY are connected by RGMII.

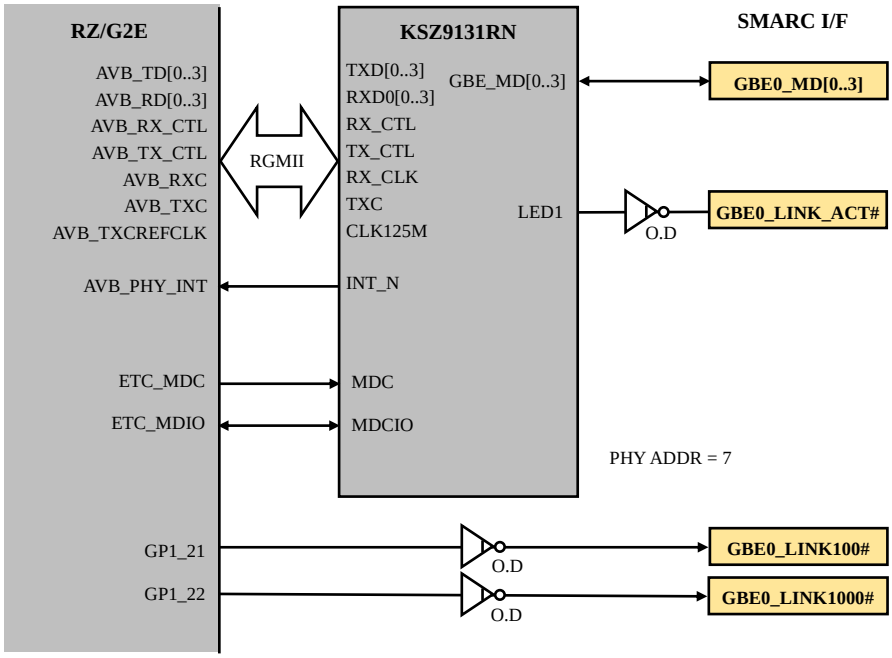


Fig 3.2-1 Gigabit Ethernet circuit connection configuration

“GBE_LINK_ACT#” is controlled by the PHY function.

“GBE_LINK100#” and “GBE_LINK1000#” are connected to the RZ/G2E port and controlled by software.

See the “KSZ9131RN (Microchip)” datasheet for information on compatible transformers.

3.3 CAMERA

CAMERA supports MIPI CSI-2 (2-lane) x 1 channel.

It is connected to CSI2 RZ/G2E and supports a maximum transfer rate of 1.1 Gbps.

The supported input formats are YUV422 8/10bit, RGB888, Embedded 8bit, and User Defined 8bit.

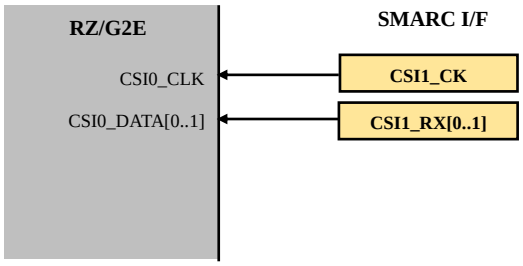


Fig 3.3-1 CAMERA circuit connection configuration

3.4 I2C

I2C, supports 4 slave channels with I2C x 3 port.

It is connected to the RZ/G2E IIC Bus Interface (I2C).

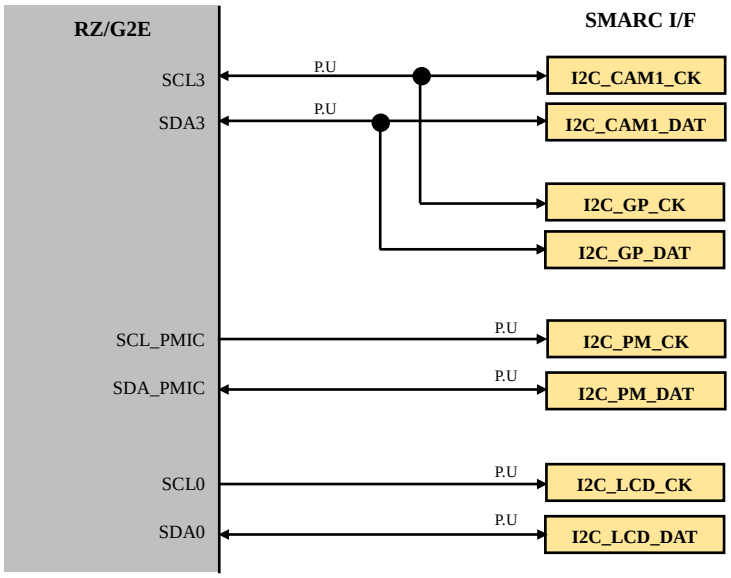


Fig 3.4-1 I2C circuit connection configuration

3.5 SDIO

SDIO supports 1 channel.

It is connected to the RZ/G2E SD card interface (SDHI), and SDCLK supports up to 200 MHz (SDR104).

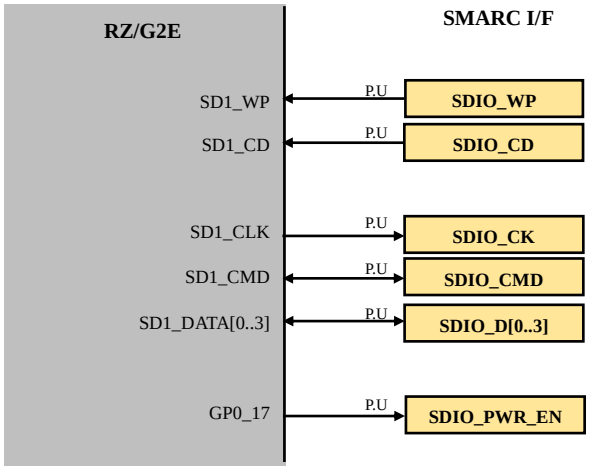


Fig 3.5-1 SDIO circuit connection configuration

3.6 AUDIO I2S

AUDIO I2S supports 1 channel.

It is connected to the RZ/G2E Serial Sound Interface (SSIU).

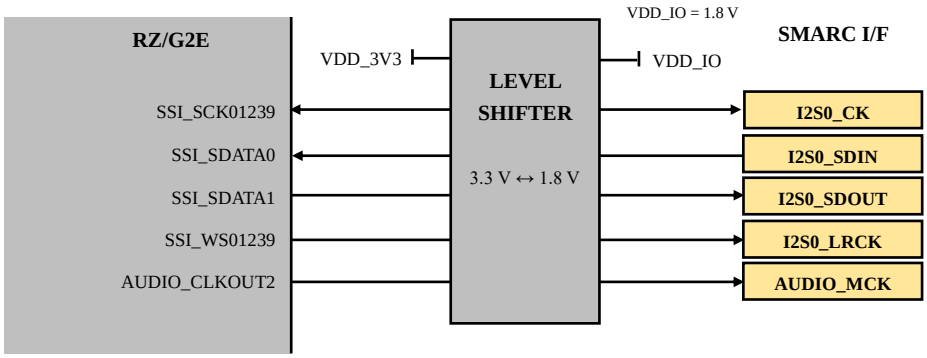


Fig 3.6-1 AUDIO I2S circuit connection configuration

The I2S signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

3.7 SPI

SPI supports 1 channel.

It is connected to the RZ/G2E Clock-Synchronized Serial Interface with FIFO (MSIOF).

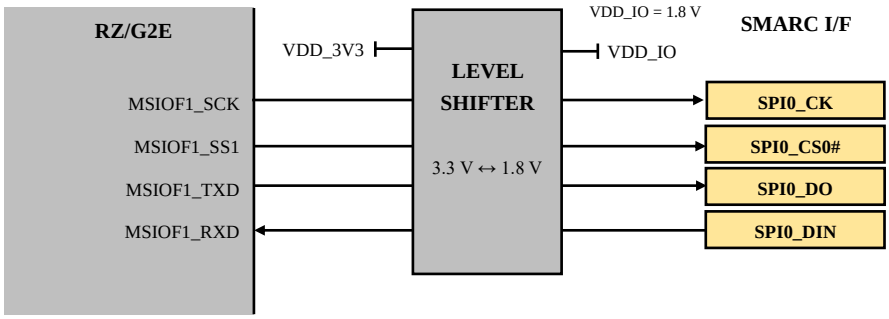


Fig 3.7-1 SPI circuit connection configuration

The SPI signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

3.8 USB 2.0

USB 2.0 supports 1 channel.
It is controlled with the RZ/G2E USB 2.0 Host (EHCI/OHCI) and USB-High-Speed Module (HS-USB).

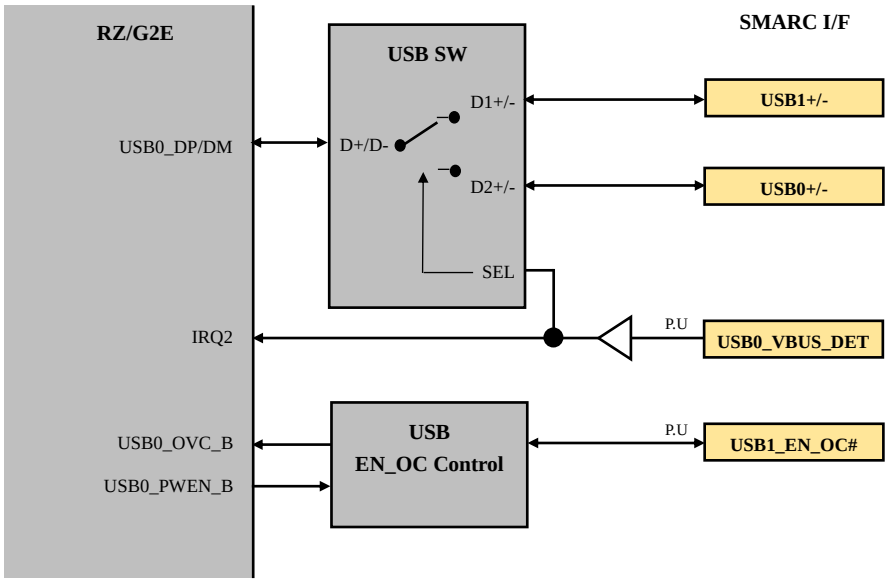


Fig 3.8-1 USB 2.0 circuit connection configuration

The RZ/G2E USB0 port is connected to USB0 (Function) and USB1 (Host) of the SMARC interface via a USB switch.
USB0 and USB1 are automatically switched. When USB0 is detected (USB0_VBUS_DET = High), it is connected to USB0.
When USB0 is not detected (USB0_VBUS_DET = Low), it will be connected to USB1.

The USBx_EN_OC# signal is input as a pulse signal when Over Current is detected, and is input to RZ/G2E by the EN_OC Control circuit as follows.

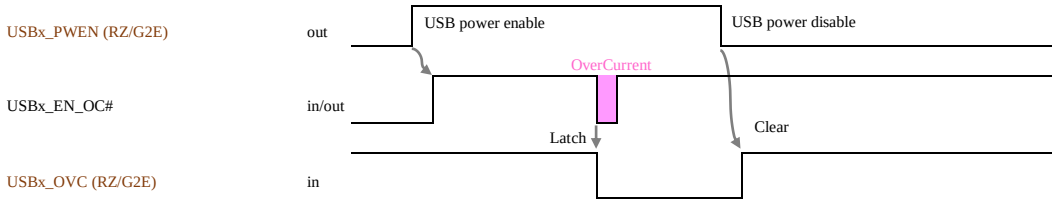


Fig 3.8-2 USBx_ENC_OC# control

USBx_OVC is held active (Low) at the falling edge of USBx_EN_OC# (overcurrent detection), and cleared (High) when USBx_PWEN is released.

3.9 USB 3.0

USB 3.0 supports 1 channel.
It is connected to the RZ/G2E USB 3.0 Host Controller.

It supports USB 3.0 DRD (Dual-role Device), and works with both HOST and Function.
Host supports Super-speed (5 Gbps), High-speed (480 Mbps), Full-speed (12 Mbps), Low-speed (1.5 Mbps).
Function supports Super-speed (5 Gbps), High-speed (480 Mbps), Full-speed (12 Mbps).

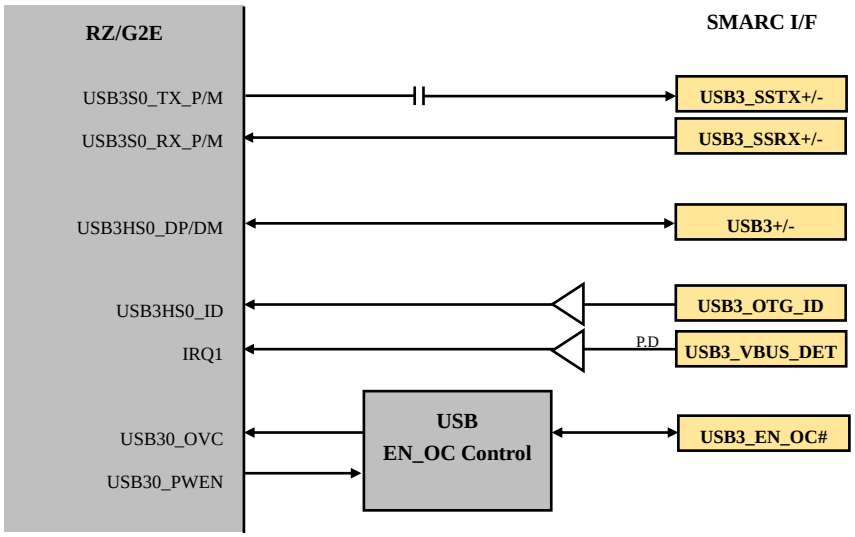


Fig 3.9-1 USB 3.0 circuit connection configuration

The RZ/G2E USB3.0 port consists of a Super-speed USB3S0 port and High-speed, Full-speed, and Low-speed USB3HS0 ports.

See Figure 3.8-2 for the USBx_EN_OC# signal.

3.10 Serial Port

Serial Port supports 3 channels.

It is connected to the RZ/G2E High Speed Serial Communication Interface with FIFO (HSCIF).

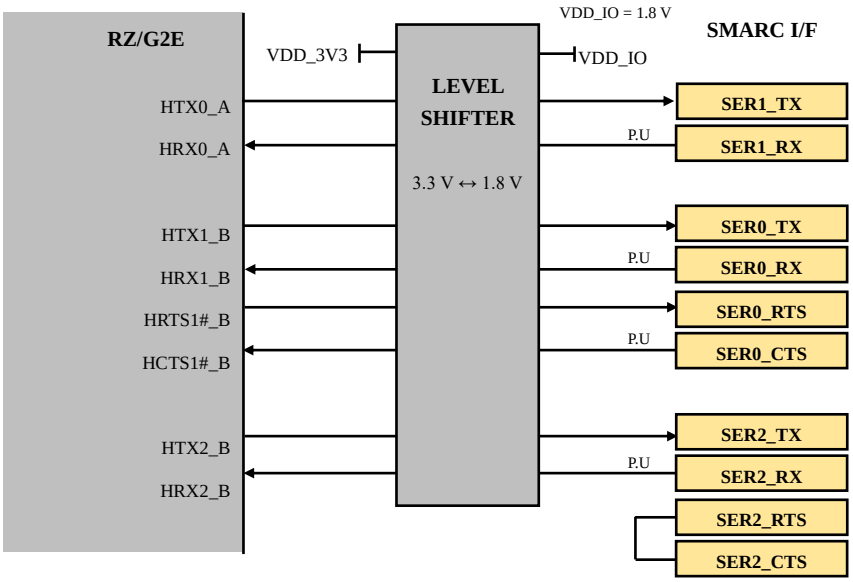


Fig 3.10-1 Serial Port circuit connection configuration

The Serial Port signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

3.11 CAN BUS

CAN BUS supports 2 channels.

It is connected to the RZ/G2E Controller Area Network Interface (CAN Interface) and CAN-FD Interface.

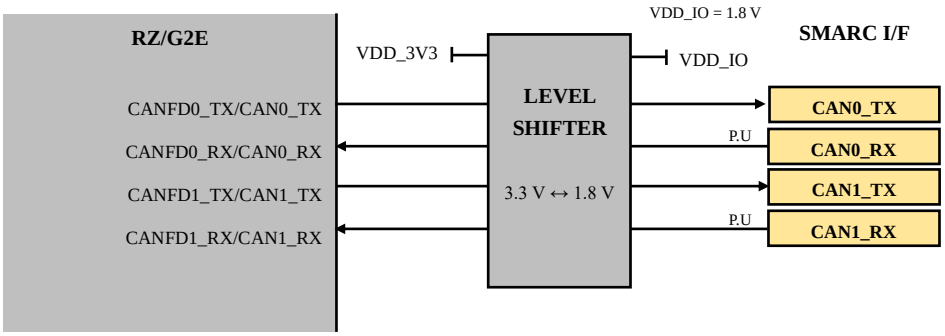


Fig 3.11-1 CAN BUS circuit connection configuration

The CAN BUS signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

3.12 PCI Express

PCI Express supports 1 lane x 1 channel.

It is connected to the RZ/G2E PCIE Controller.

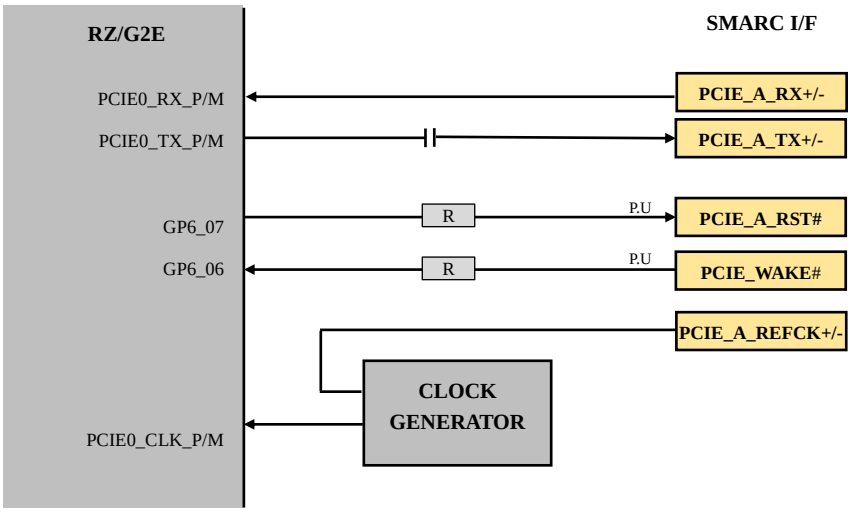


Fig 3.12-1 PCI Express circuit connection configuration

3.13 GPIO

GPIO supports 14 ports.

It is connected to the RZ/G2E General-Purpose Input/Output Ports (GPIO).

GPIO can set input/output for each port.

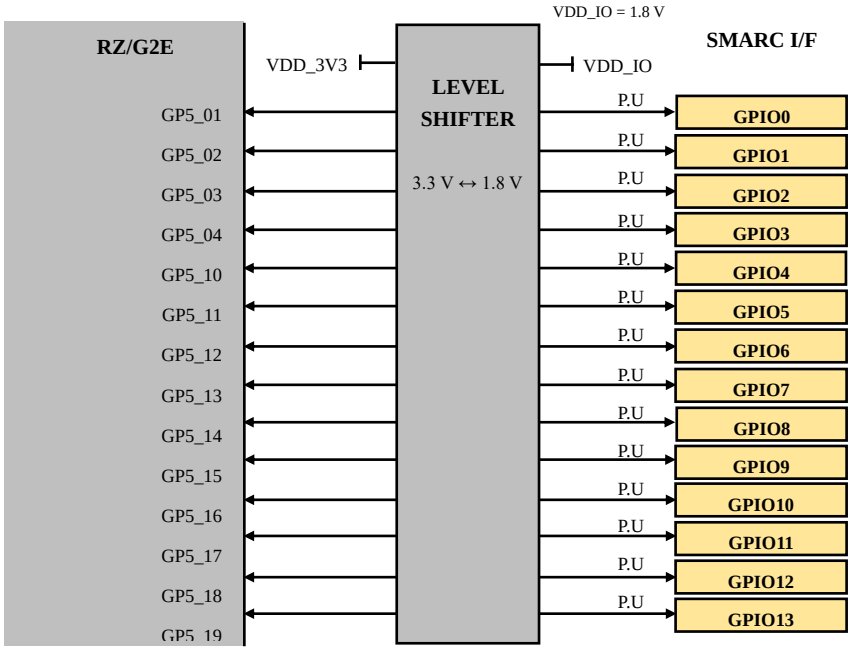


Fig 3.13-1 GPIO circuit connection configuration

The GPIO signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

The RZ/G2E GPIO port assigned to GPIO is a combination terminal with the interface function, so it can be used for purposes other than GPIO.

Below are some of the functions of the combination terminal. (See the RZ/G2E datasheet for details)

Note that non-GPIO functions are not standard in the SMARC standard.

SMARC GPIO	RZ/G2E GPIO	Interface Function		
		SCI	MSIOF	SSI
GPIO0	GP5_01	RX0		
GPIO1	GP5_02	TX0		
GPIO2	GP5_03	CTS0		AUDIO_CLKOUT
GPIO3	GP5_04	RTS0		AUDIO_CLKOUT1
GPIO4	GP5_10		MSIOF0_SCK	SSI_SCK78
GPIO5	GP5_11	TX2	MSIOF0_RXD	SSI_WS78
GPIO6	GP5_12	RX2	MSIOF0_TXD	SSI_SDATA7
GPIO7	GP5_13		MSIOF0_SYNC	SSI_SDATA8
GPIO8	GP5_14		MSIOF0_SS1	
GPIO9	GP5_15		MSIOF0_SS2	
GPIO10	GP5_16			AUDIO_CLKC
GPIO11	GP5_17	RX0		
GPIO12	GP5_18	SCK0		
GPIO13	GP5_19	TX0		

Table 3.13-2 GPIO combination terminal function

4. Power Supply and System Control

4.1 Power Supply

The main power supply of this module is input from VDD_IN and is designed to be fixed at 5 V.
RTC can be backed up from VDD_RTC.

Signal Name	Input/Output	Function
VDD_IN	Input	Main power input 4.75 V to 5.25 V Current: Typ 500 mA / Max 2A (equipped with αSMARC-EVB1, no external connection)
VDD_RTC	Input	Power supply for RTC backup: 2.0 to 3.3 V Backup period: Reference 15 years or more when using CR2012 (3.0 V / 55 mA)

Table 4.1-1 Power Supply Input

The current consumption of the module (VDD_IN) varies depending on the application.
In most use cases, the average current consumption is less than 5 W (1 A @ 5 V), In applications that handle multimedia such as video, current consumption increases momentarily, so supply a maximum of 10 W (2 A @ 5 V).

4.2 System Control

4.2.1 RESET

RESET_IN# is driven from the carrier board, putting the module in the reset state.
RESET_OUT# is the reset output to the carrier board.

Signal Name	Input/Output	Function
RESET_IN#	Input	RESET input signal Module is in reset state during the Low period.
RESET_OUT#	Output	RESET output signal Low active reset output to the carrier board.

Table 4.2-1 RESET signal

4.2.2 FORCE_RECOV

The FORCE_RECOV# signal is used for firmware updates.

Signal Name	Input/Output	Function
FORCE_RECOV#	Input	Forced recovery signal When the module is started with FORCE_RECOV# set to Low, it boots from SPI FLASH.

Table 4.2-2 FORCE_RECOV# signal

4.2.3 Power Supply Control

The power supply control signal supports the following signals.

Signal Name	Input/Output	Function
CARRIER_PWR_ON	Output	Power ON signal to carrier board The carrier board circuits should not be powered up until this signal is High.
VIN_PWR_BAD#	Input	Power status signal from the carrier board The module and carrier board should not be powered up during this signal is Low.
POWER_BTN#	Input	Power button input signal from the carrier board When the power button is pressed, it turns Low, and power to the module is turned on.

Table 4.2-3 Power Supply Control Signal

In addition to the above signals, power control is controlled by software using the RZ/G2E ports listed below.

Port Name	Input/Output	Function
GP1_00/IRQ0	Input	POWER_BTN# input Detect input of POWER_BTN#
GP6_08	Output	Module power supply control output During the High period, the power supply in the module is on. When it is Low, the power inside the module is turned off.

Table 4.2-4 Power Supply Control Signal

The connection configuration of the power supply part is shown below.

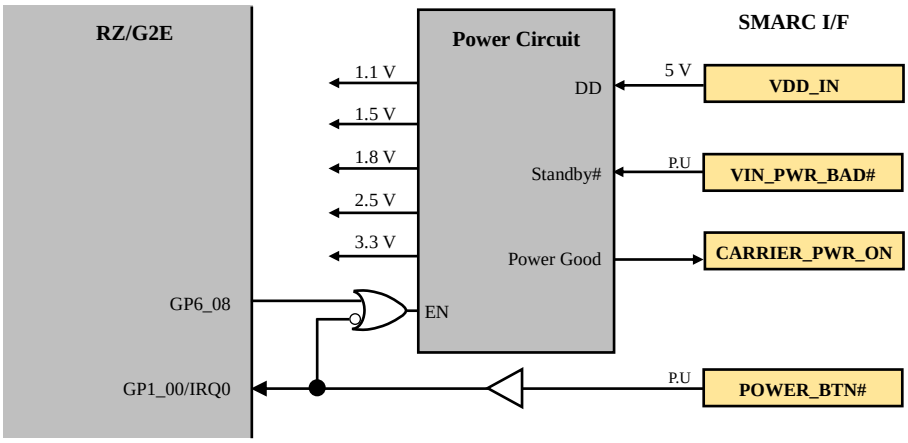


Fig 4.2-5 Power supply connection configuration

The power supply of this module is controlled according to the following sequence.

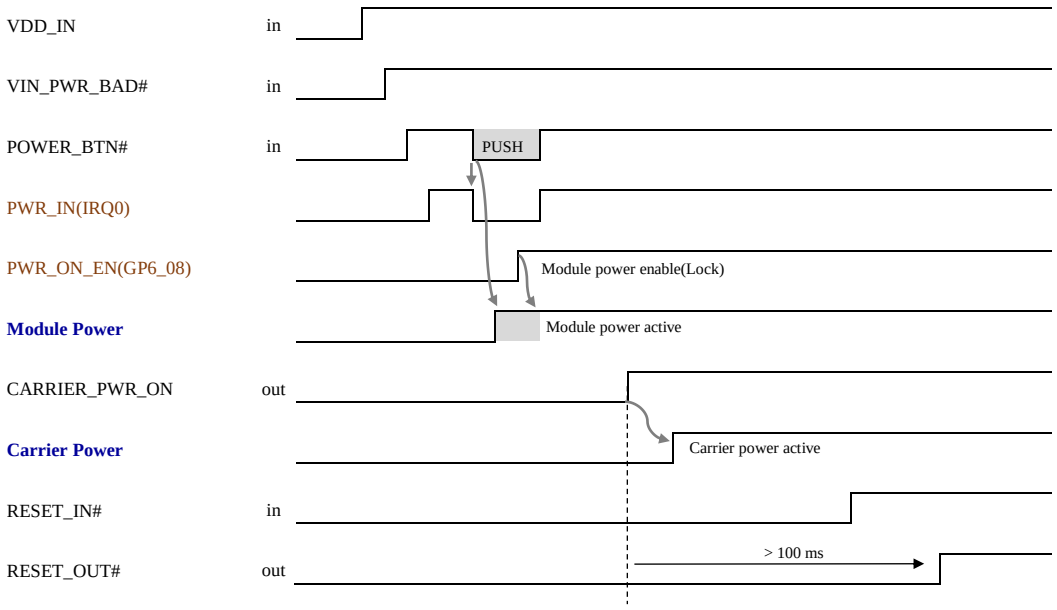


Fig 4.2-6 Power supply control sequence

4.2.4 BOOT_SEL

The BOOT_SEL signal is connected to the RZ/G2E port input.
With this module, the initial boot is done from eMMC regardless of the setting of the BOOT_SEL signal, so there is no problem even if everything is open.

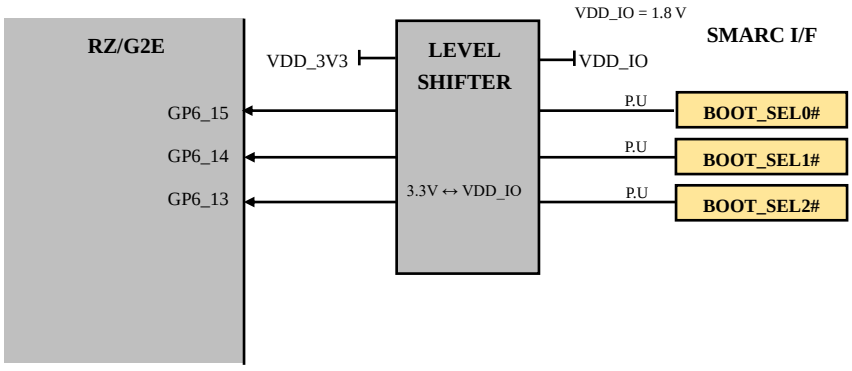


Fig 4.2-7 BOOT_SEL# circuit connection configuration

The BOOT_SEL signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

4.2.5 TEST

The TEST signal is connected to the RZ/G2E port input.

With this module the TEST function is not supported, so there is no problem if it is not used.

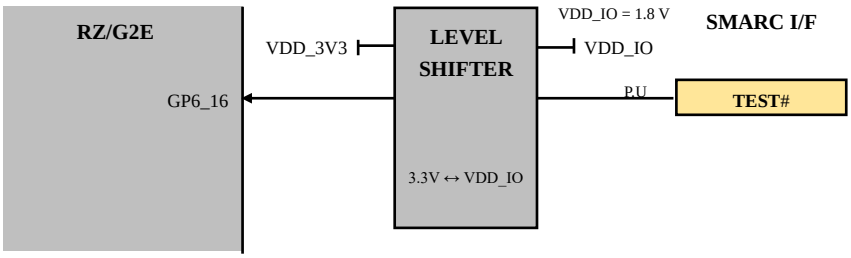


Fig 4.2-8 TEST circuit connection configuration

The TEST signal is relayed through the LEVEL SHIFTER and bi-directionally converted to 3.3 V and VDD_IO.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “2.5.2 VDD_IO Settings”.

5. Technical Data

5.1 External Dimensions

5.1.1 Module External Dimensions

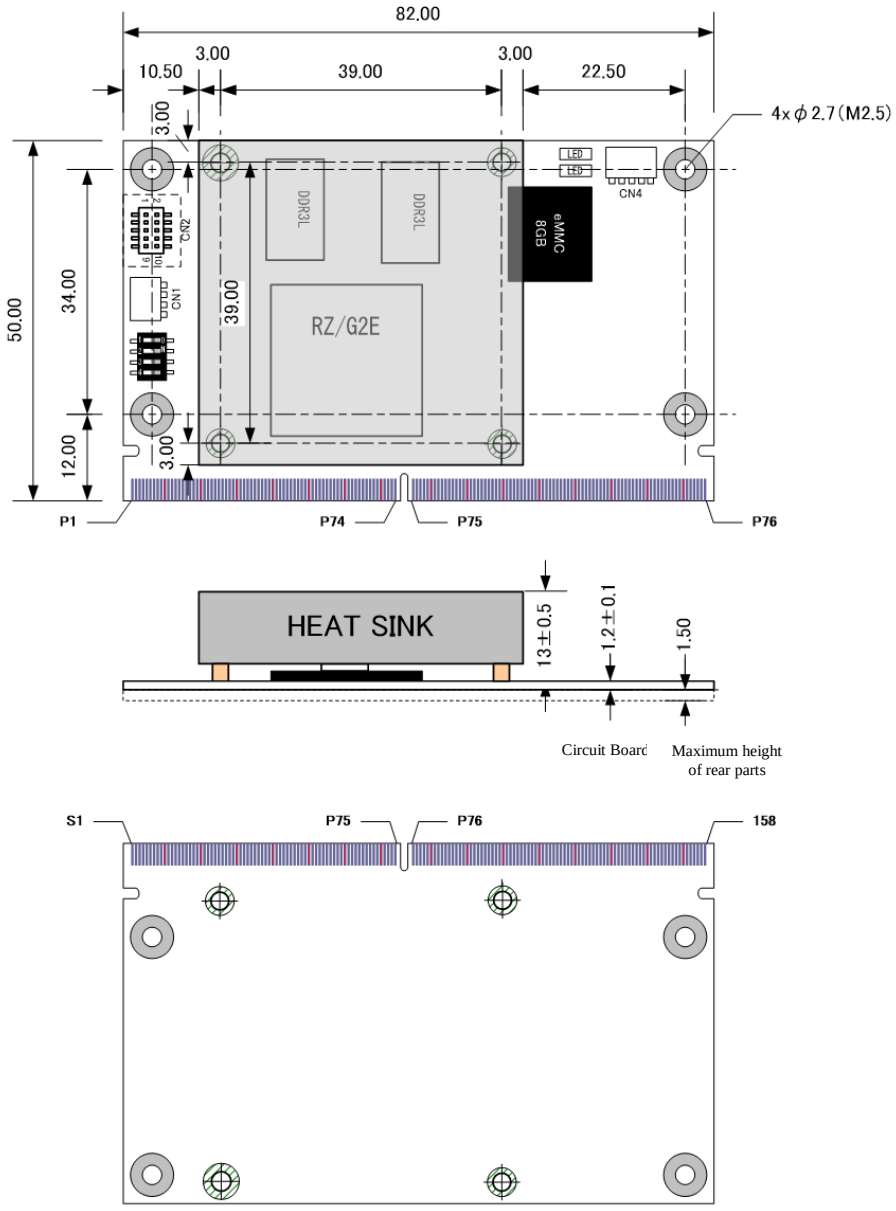


Fig 5.1-1 αSMARC-RZ/G2E dimensional drawing

For more detailed external dimensions, see the SMARC standard specifications.

SMARC Hardware Specification 2.1.1 https://www.sget.org/standards/smarc/

5.1.2 Carrier Board Footprint

For carrier board footprint information, see the SMARC standard specification.

Excerpt from SMARC 2.1.1 Specification

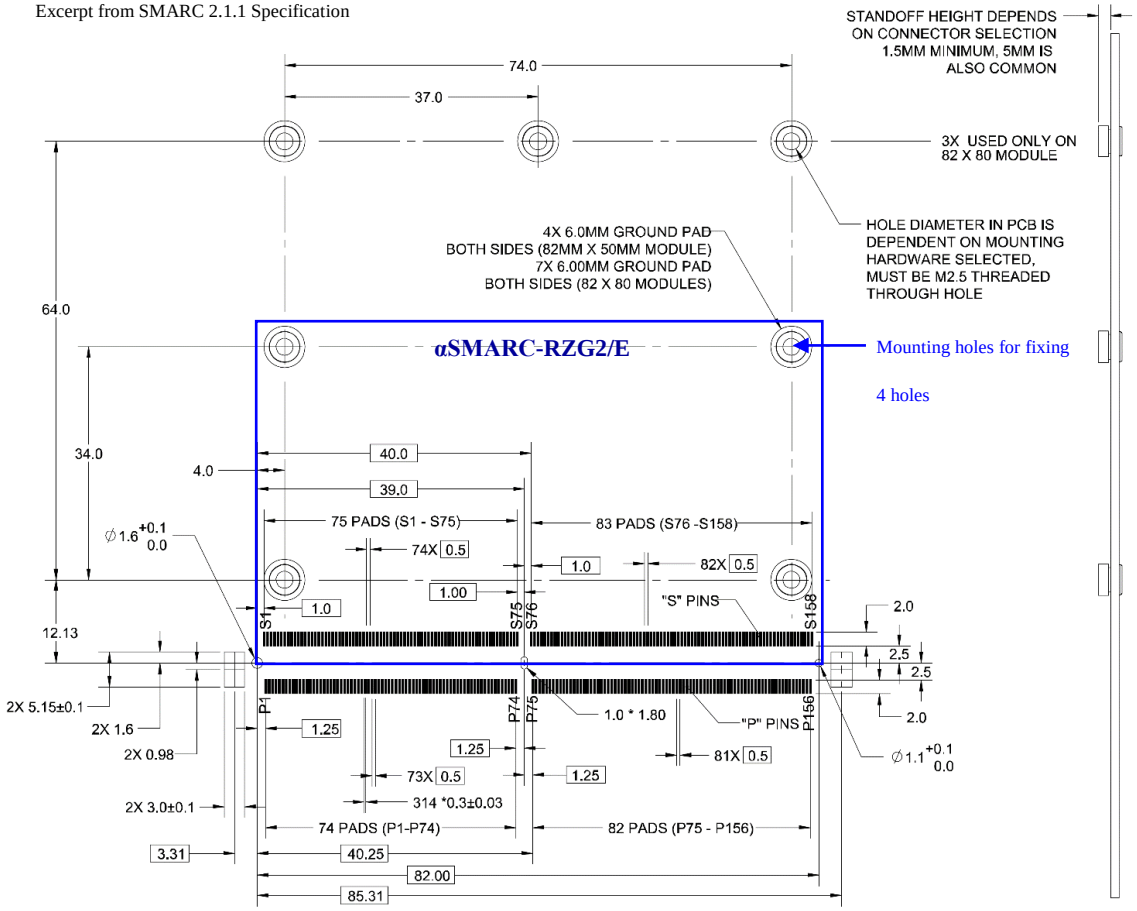


Fig. 5.1-2 Carrier board footprint

5.1.3 Standoff

For the mounting holes for fixing, implement a tapped standoff on the carrier board side and screw it down.

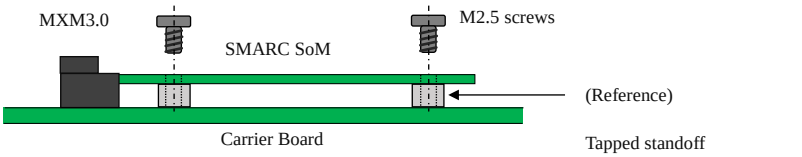


Fig 5.1-3 SoM standoff

5.2 Compatible Connectors

5.2.1 MXM3.0 Card Edge Connector

SMARC SoM is compatible with MXM3.0 connectors (314 pin).
See the SMARC standard specifications for recommended connector model numbers.

5.2.2 Installation to Carrier Board

Install a SMARC module by plugging it into a card edge connector on the carrier board.
The card edge connector is fragile, so handle it with adequate care.
Also, be careful not to allow dust or foreign objects to get caught in the contact area of the card-edge.

[Installation Method]

1. Insert the SMARC module diagonally (at an angle of about 30°) into the card edge connector of the carrier board.
2. With the SMARC module inserted into the card edge connector, push it down so that it is parallel to the carrier board.
3. Secure the SMARC module with screws.

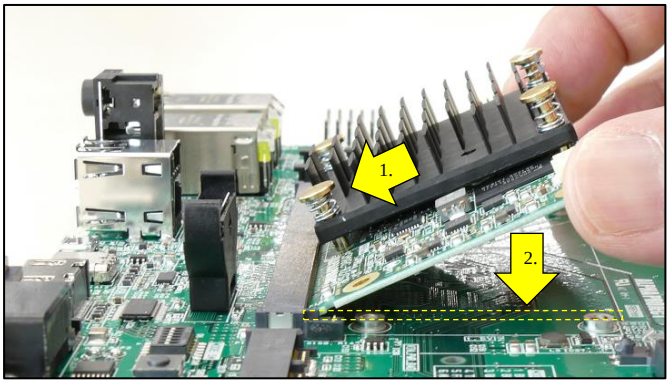


Fig 5.2-1 Installation to carrier board

5.3 Designing the Carrier Board

5.3.1 Design Reference

Refer to the guidelines published by SGeT regarding the design of the carrier board.
Refer to this manual for the functions and restrictions specific to this board.

SMARC Design Guide Ver. 2.1.1 https://www.sget.org/standards/smarc/

A SMARC2.1 standard compliant carrier board “αSMARC-EVB1” is available for evaluation.
The circuit diagram of the carrier board has been published, so it can be used for design reference and performance evaluation.

5.3.2 Notes and Restrictions

Consider the following notes and restrictions when designing carrier boards.

1. About VDD_IO system signals
   For VDD_IO system signals, the output resistance of the LEVEL SHIFTER is about 4 Kohm, so we recommend 50 Kohm or more when connecting a pull-up or pull-down resistor to the output signal.
   Design the capacitive load to be 70 pF or less.
   Drive the input signal with a driver that has a maximum drive capacity of 2 mA.

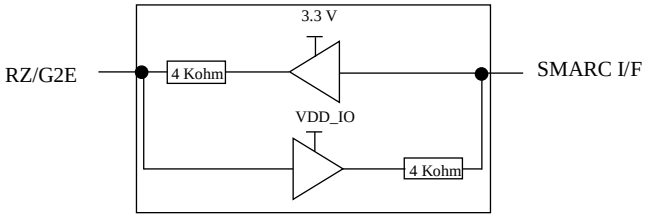


Fig 5.3-1 LEVEL SHIFTER equivalent circuit

2. Signal delay of VDD_IO system signals
   The VDD_IO system signal has a delay because it relays through the LEVEL SHIFTER.
   Consider this when using a clock synchronous interface such as SPI or I2S.

Input/Output	VDD_IO = 1.8 V		VDD_IO = 3.3 V	
	MIN	MAX	MIN	MAX
Input	1.6 ns	11 ns	1.3 ns	6.8 ns
Output	1.5 ns	12 ns	0.8 ns	7.6 ns

Table 5.3-2 VDD_IO system signal delay

3. Impedance matching
   Do impedance matching according to each standard for the PCB patterns of high-speed interface signals such as Ethernet, USB, PCIe, and LVDS.

4. About ESD countermeasures
   Each signal of the SMARC interface is not subject to ESD countermeasures on the module.
   Take these measures as necessary on the carrier board.

5.4 Heat Dissipation Measures

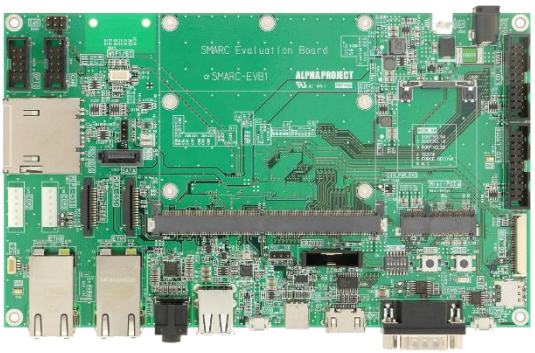
This module is equipped standard with a natural air-cooling heat sink, so additional measures such as fans are not required in environments where there is air convection.

However, heat dissipation should be considered when using it in sealed enclosures or high temperature environments.

6. Related Products

6.1 SMARC2.1 Compliant Carrier Board

"αSMARC-EVB1" is a carrier board that conforms to the SMARC2.1 standard.
It can be used for SMARC module evaluation, application development and prototyping purposes.
Also, the circuit diagram has been published, so it can be used as a reference for carrier board design.



αSMARC-EVB1

6.2 αSMARC-RZ/G2E Development Kit

"αSMARC-RZ/G2E development kit" is a development kit that includes a SMARC module, carrier board, AC adapter, and Linux BSP.
It includes all the equipment and software necessary for development, so development can start right away.

αSMARC-RZ/G2E

αSMARC-EVB1

AC adapter

6.3 Card Edge Connector

Alpha Project can provide MXM3.0 card edge connectors that are compatible with SMARC modules.
Please inquire with us.

7. Product Support Information

Alpha Project's product support accepts user registration, repairs, inquiries, etc. See the page below for information.

Product Support Page*

https://www.apnet.co.jp/support/index.html

* Japanese site only.

User Registration

Please do user registration before requesting repairs or making inquiries.

Registered users also get notices of version upgrades and the latest information by email.

Warranty & Repair Applications

Alpha Project provides initial defect replacement and free warranty in accordance with the product warranty regulations.

We offer paid repairs for products that have passed the warranty period.

You can apply from the product warranty and product repair options on the product support page.

Inquiries

We accept general questions about our products.

When you inquire, make sure to include the product name, use environment, use method, and problems in the details.

Please note that we do not accept inquiries about the following content.

- ■ Questions about the circuit operation of this product and method of using CPUs and peripheral devices
- ■ Questions about the use methods and operations of user circuits
- ■ Guidance on operation of related tools
- ■ Other questions outside the scope of product specifications and problems that should be solved by customers' technology

Please note that Alpha Project does not accept questions about customers' individual software.

Customers who wish to receive support will be served individually for a fee. See "8. Information on Engineering Services".

8. Information on Engineering Services

Alpha Project accepts orders for custom products and system development based on our products.
We provide integrated service from design to OEM supply according to customers specifications.
For details, contact our sales office.

Information on Engineering Services*

https://www.apnet.co.jp/engineering/index.html

Inquiries

sales@apnet.co.jp

* Japanese site only.

Revision History

Version Number	Date	Revision Contents
Version 1.0	July 26, 2023	Create a new entry
Version 2.0	October 2, 2023	Added description of preinstalled OS. Update address.

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